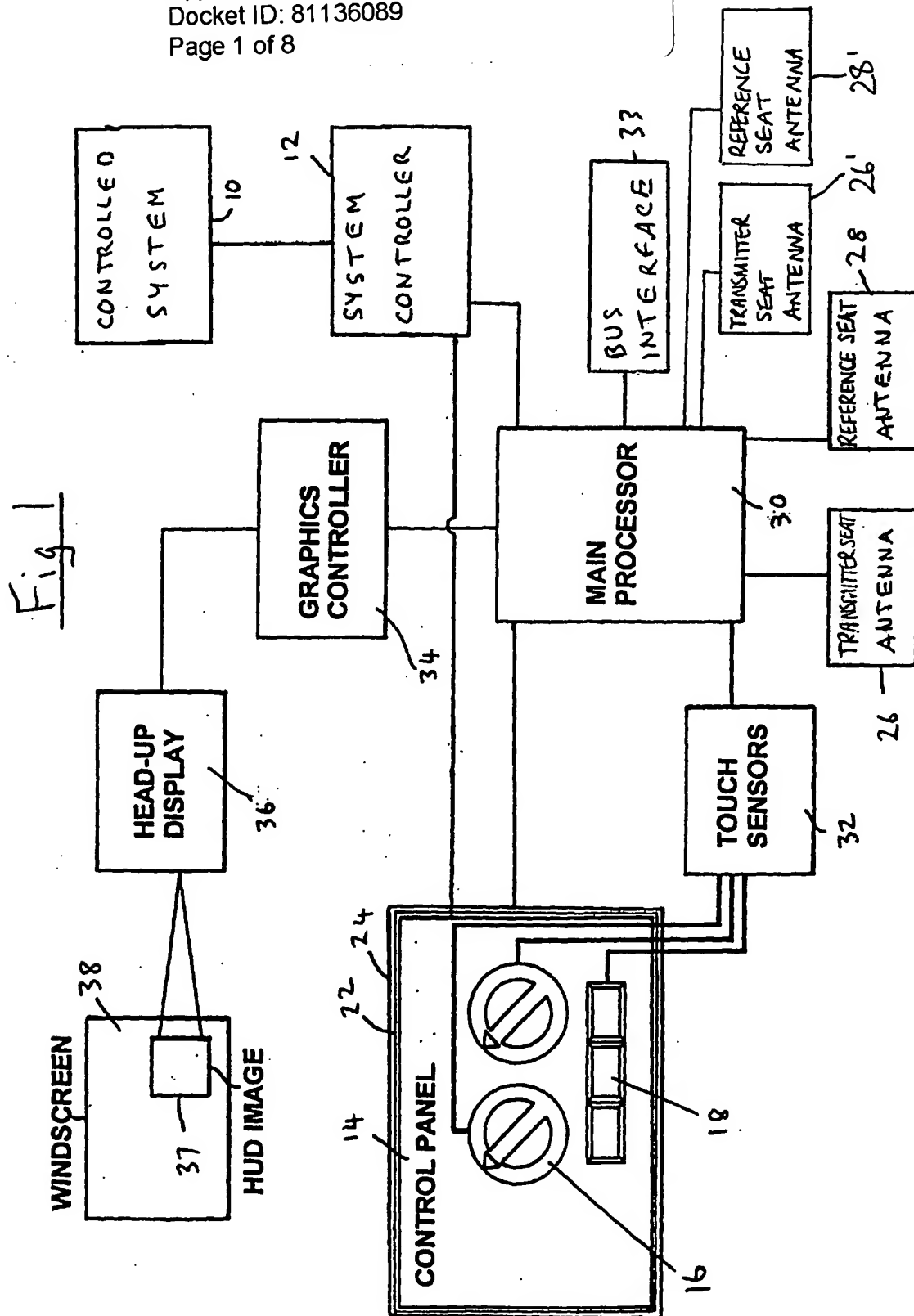


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Fig. 2

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36

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MAIN PROCESSOR

BUS INTERFACE

24

26

26s

26sp

27

28

28s

28sp

29

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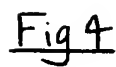
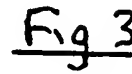
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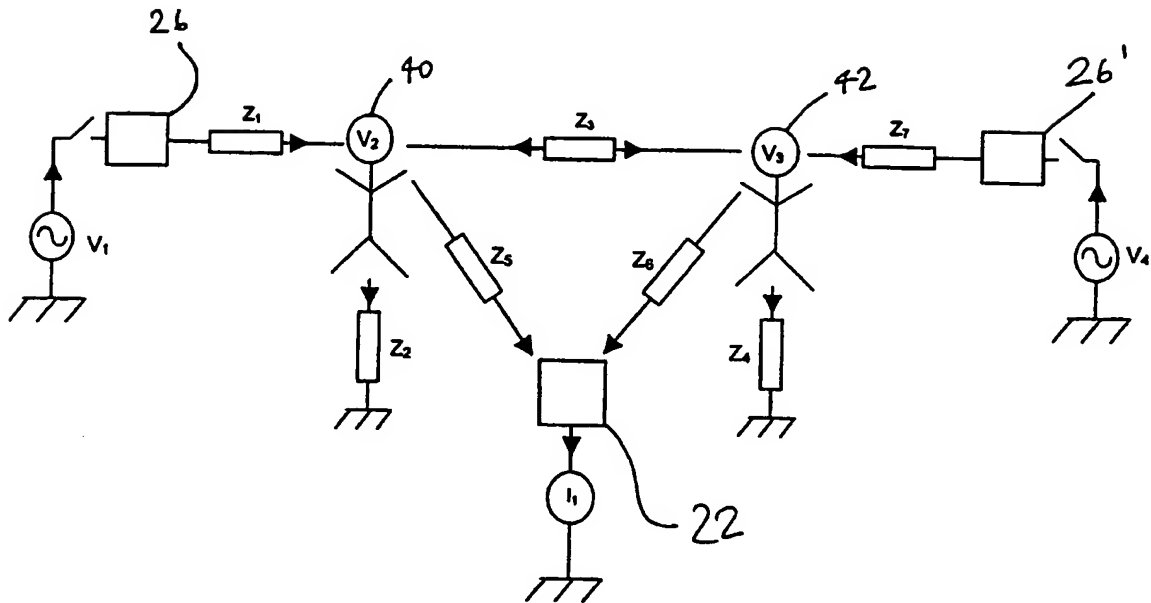


Fig 5

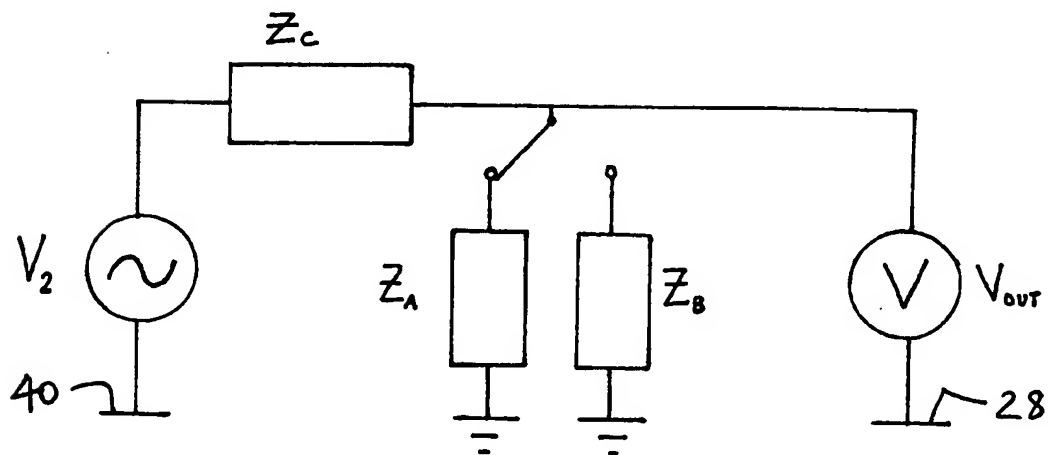


Fig 6

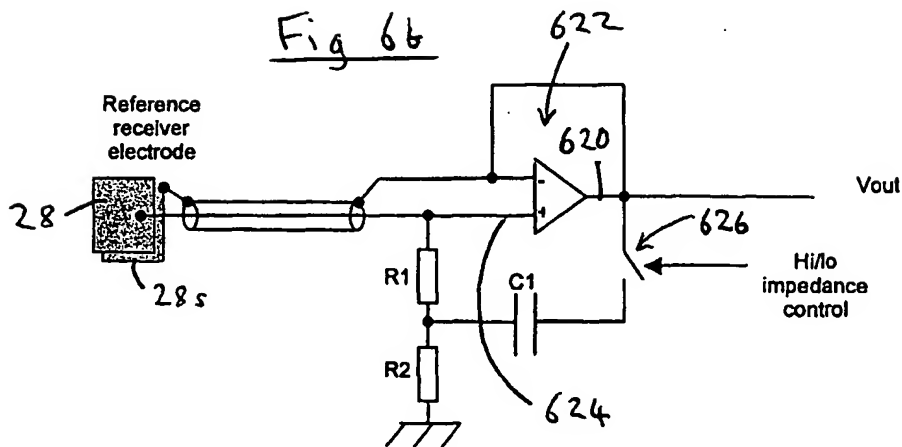
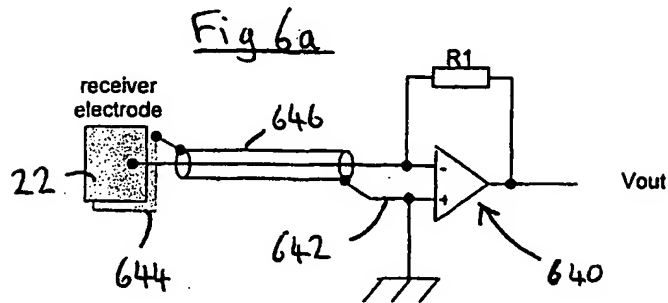
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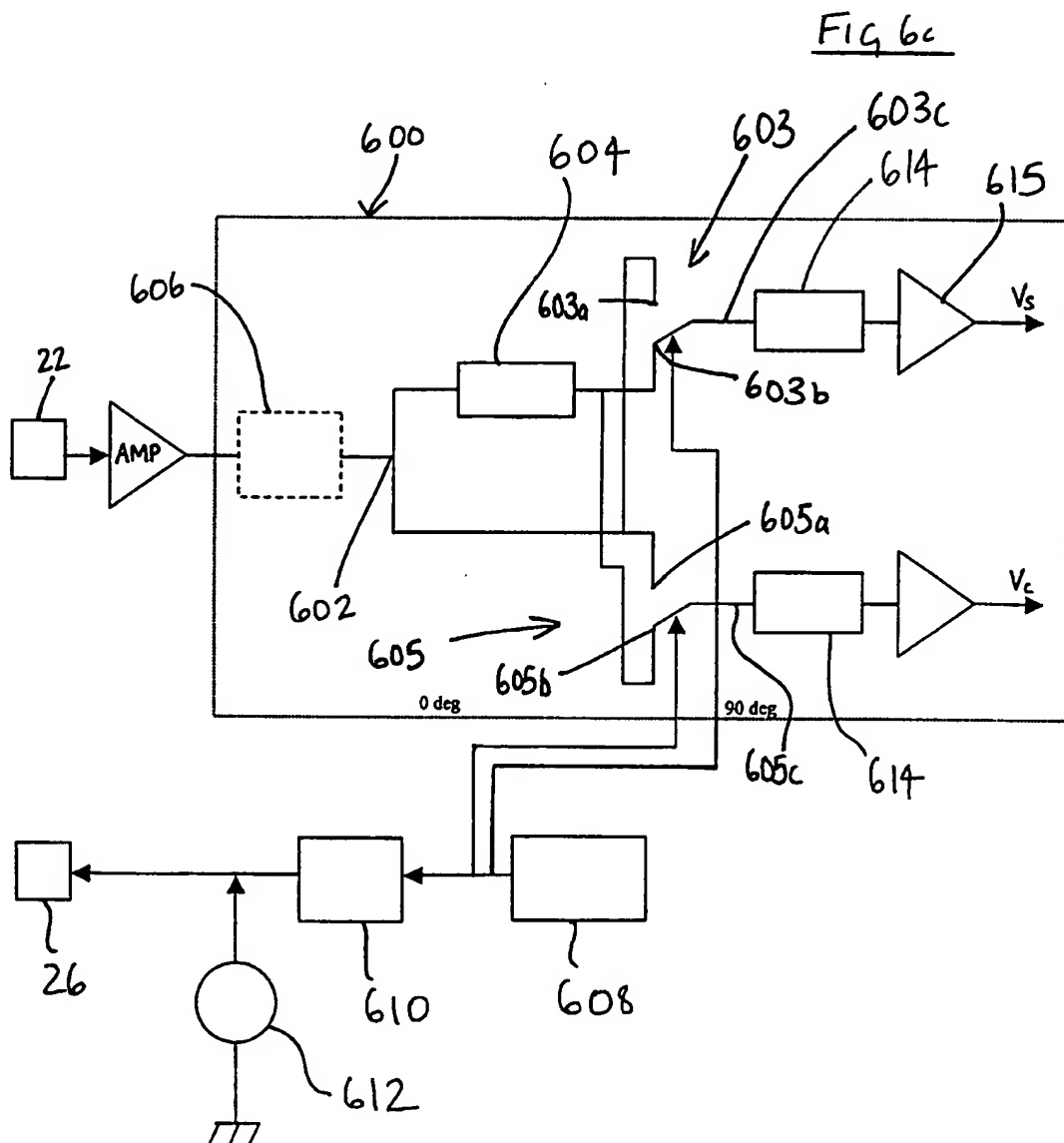


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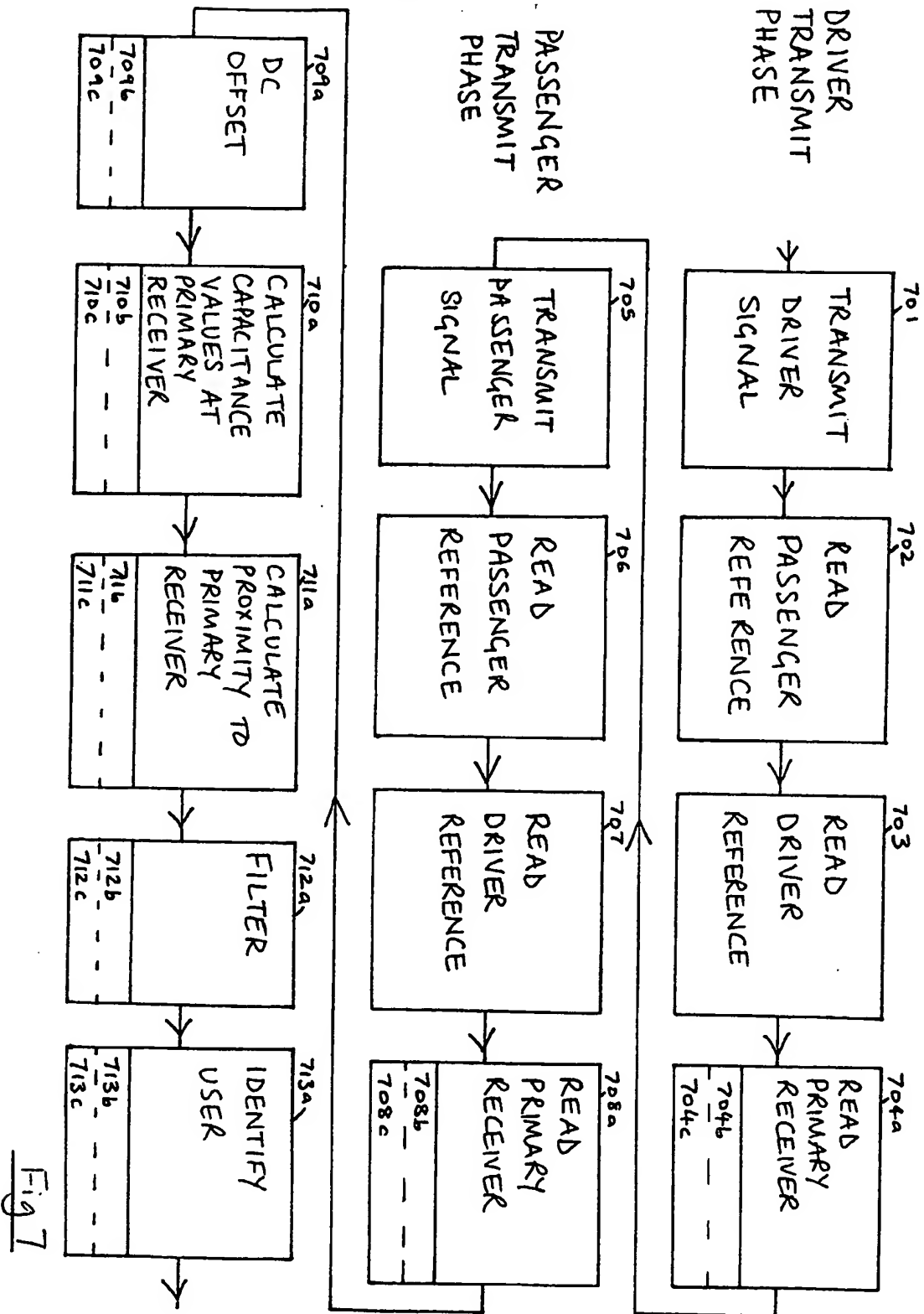


Fig 7

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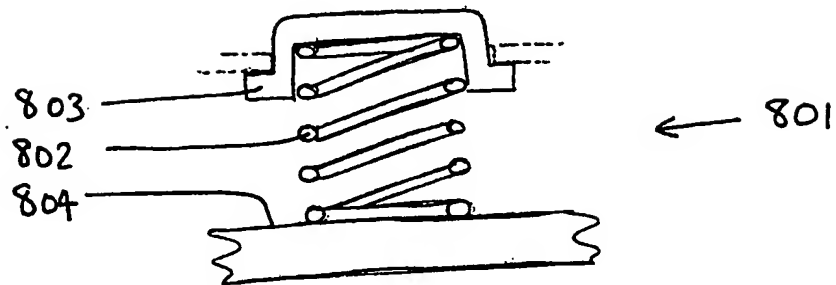


Fig 8